

PG410 A01

GP106 8GB/4GB GDDR5, 256b, 256Mx32/128MX32
Tall DVI-D + DP + DP + HDMI/DP + DP

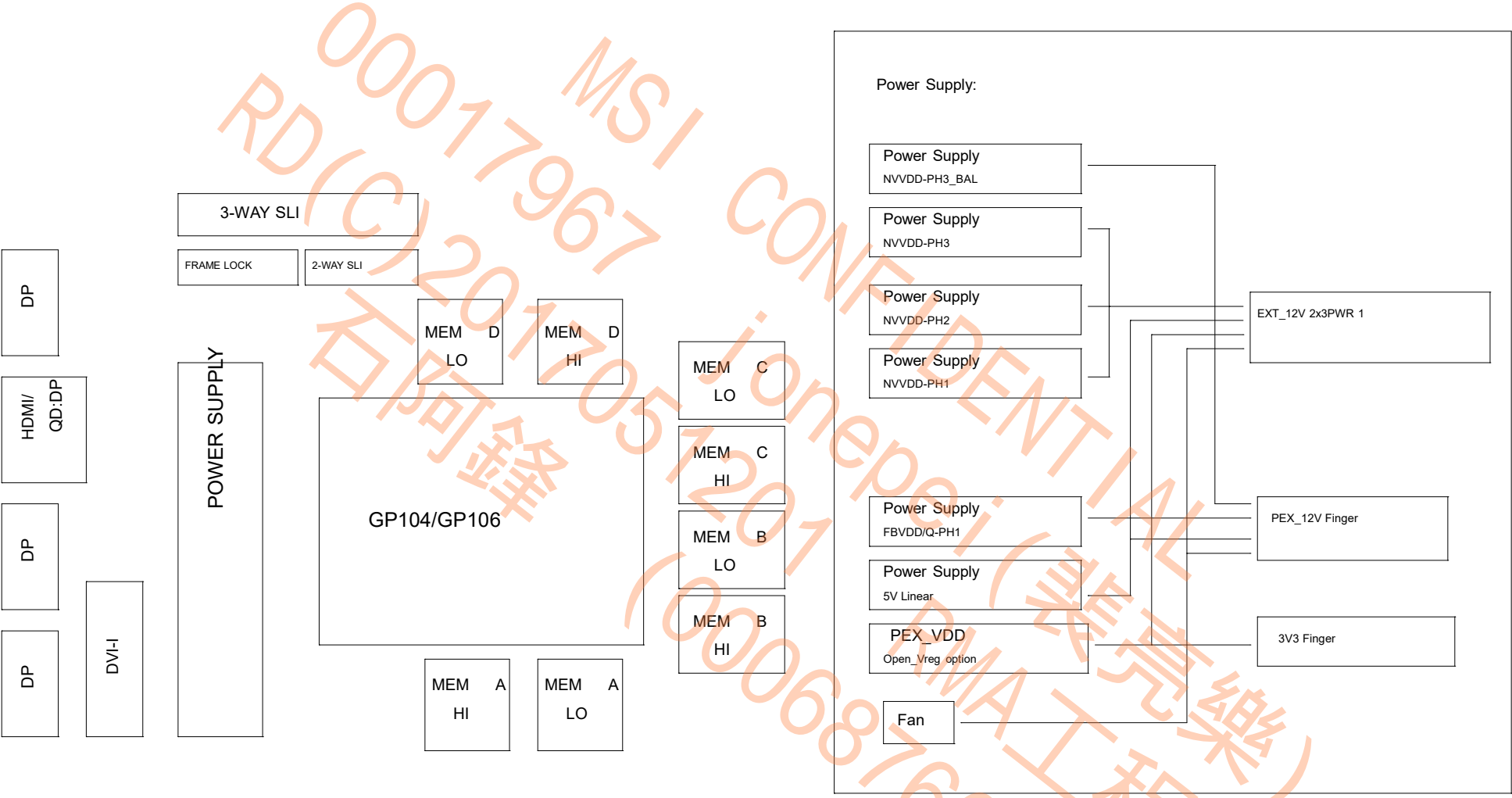
TABLE OF CONTENTS

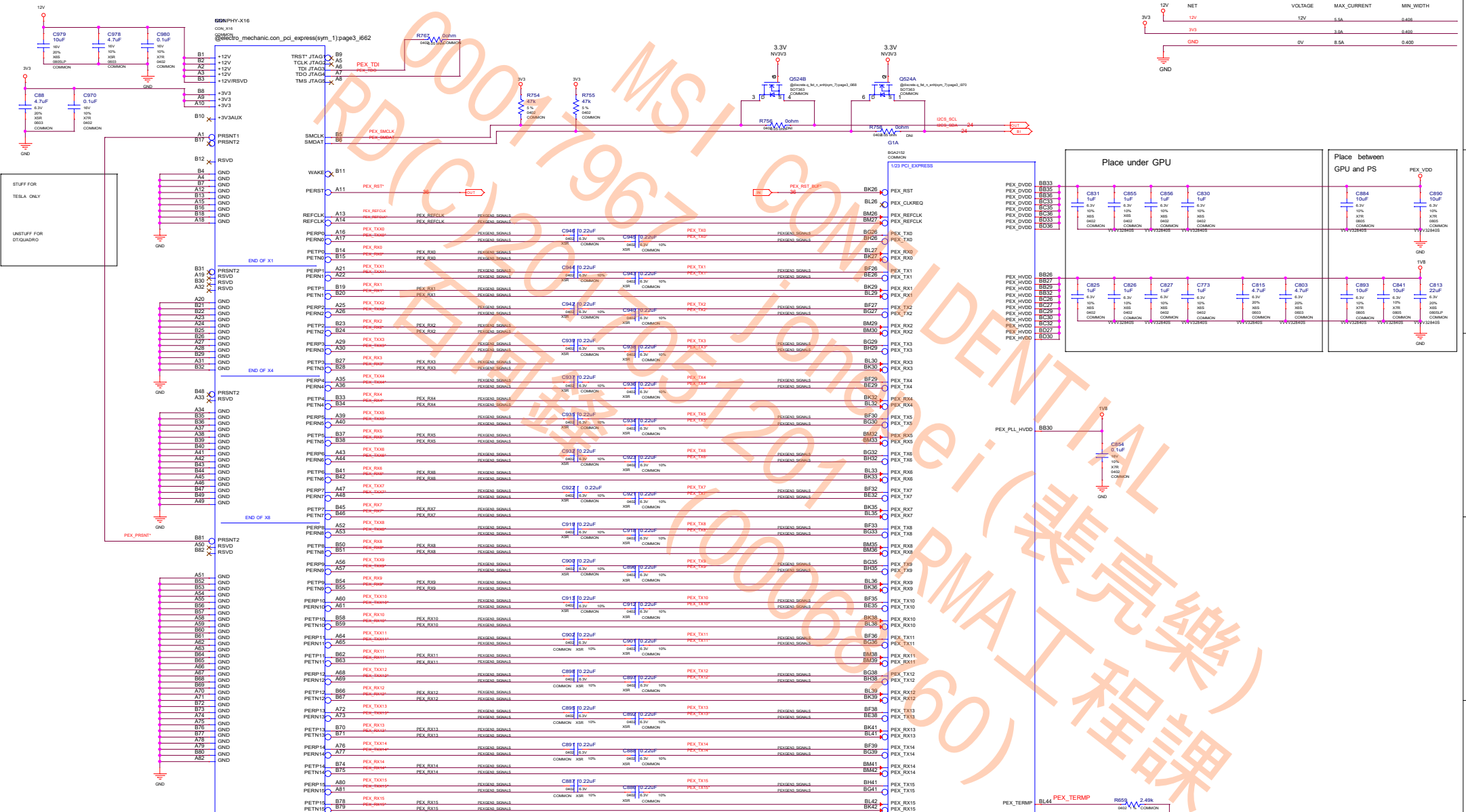
Page	Description
1	Table of Contents
2	Block Diagram
3	PCI Express
4	GPU FB_AB
5	MEMORY: FBA[31:0]
6	MEMORY: FBA[63:32]
7	MEMORY: FBB[31:0]
8	MEMORY: FBB[63:32]
9	MEM FB_AB PWR
10	GPU FB_CD
11	MEMORY: FBC[31:0]
12	MEMORY: FBC[63:32]
13	MEMORY: FBD[31:0]
14	MEMORY: FBD[63:32]
15	MEM FB_CD PWR
16	GPU PWR & GND
17	GPU Decoupling
18	IFPAB DVI-D-DL
19	IFPE DP
20	IFPF DP
21	IFPC HDMI/DP
22	IFPD DP
23	MIOA/B Interface and Frame Lock
24	MISC1: Fan, Thermal, JTAG, GPIO, STEREO
25	MISC2: ROM, XTAL, STRAPS

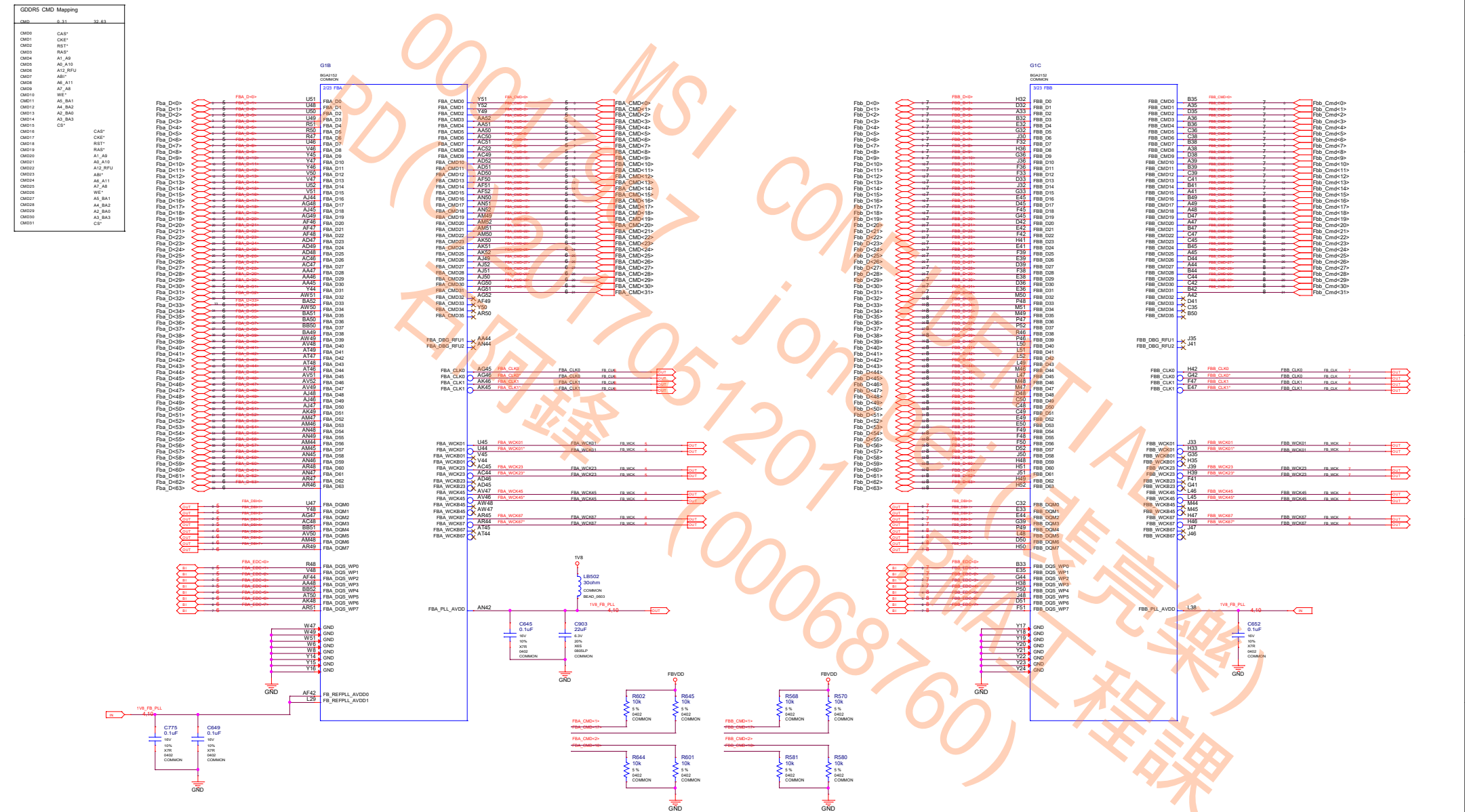
Page	Description
26	PS: 1V8_PLL, 1V8_AON
27	PS: 5V, PEX_VDD
28	PS: NV3V3, NV12V
29	PS: FBVDD
30	PS: NVVDD Controller
31	PS: NVVDD Phase 1, 2 & 3
32	PS: NVVDD Rail Balance Login & Dynamic Phase
33	PS: Input, Filtering, and Monitoring
34	PS: 12V Power Steering, PSI Control & LED
35	PS: Shut Down and Sequencing
36	PS: GC6 MISC
37	MECH

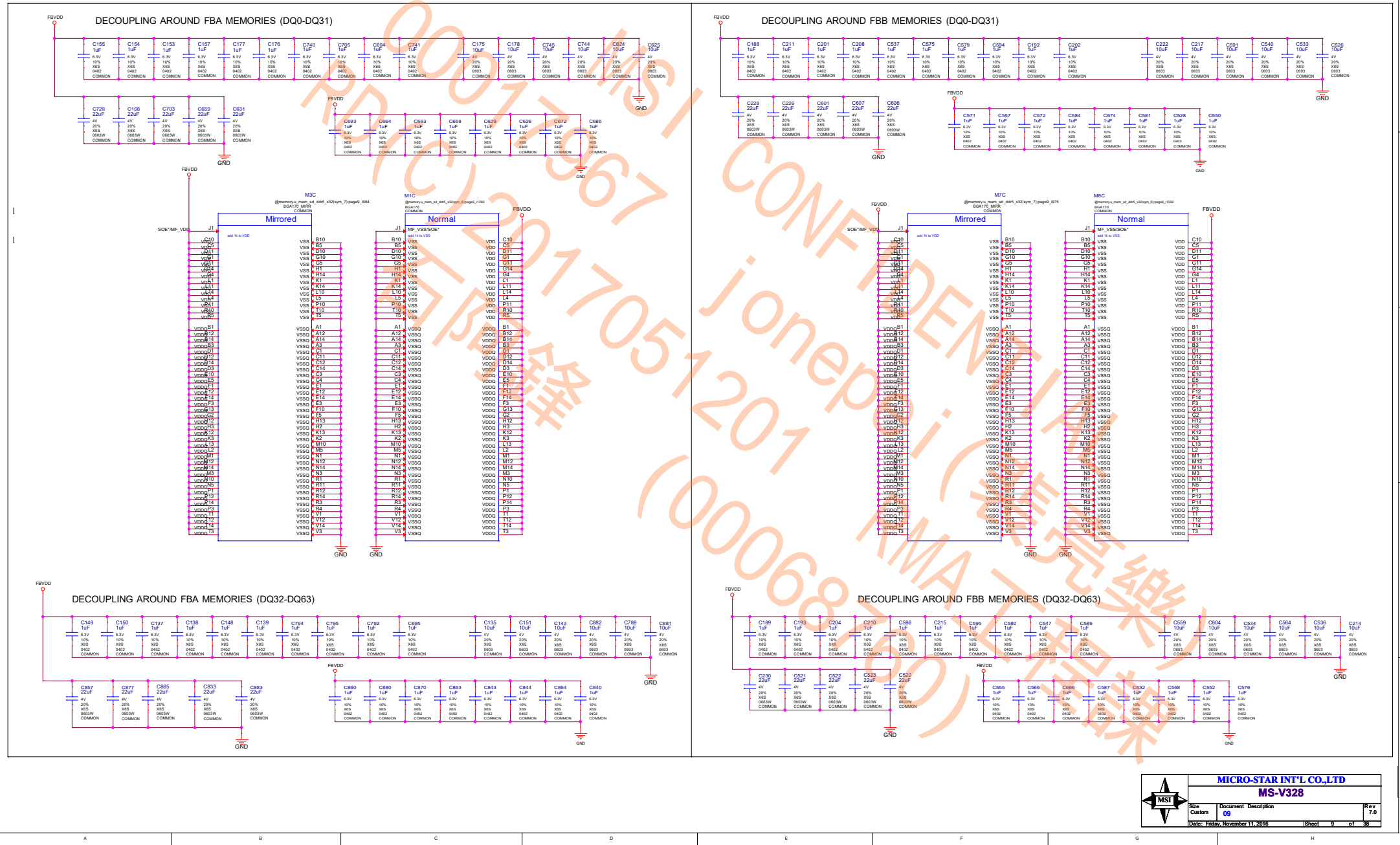
6.1
1. PS: NVVDD_VR
2. PS: L_OVR
3. PS: C_OVR
4. PS: HDMI_DP_OVR

		MICRO-STAR INT'L CO., LTD	
		MS-V328	
Size	Document	Description	Rev
Custom	01		7.0
Date: Friday, November 11, 2016		Sheet	1 of 38



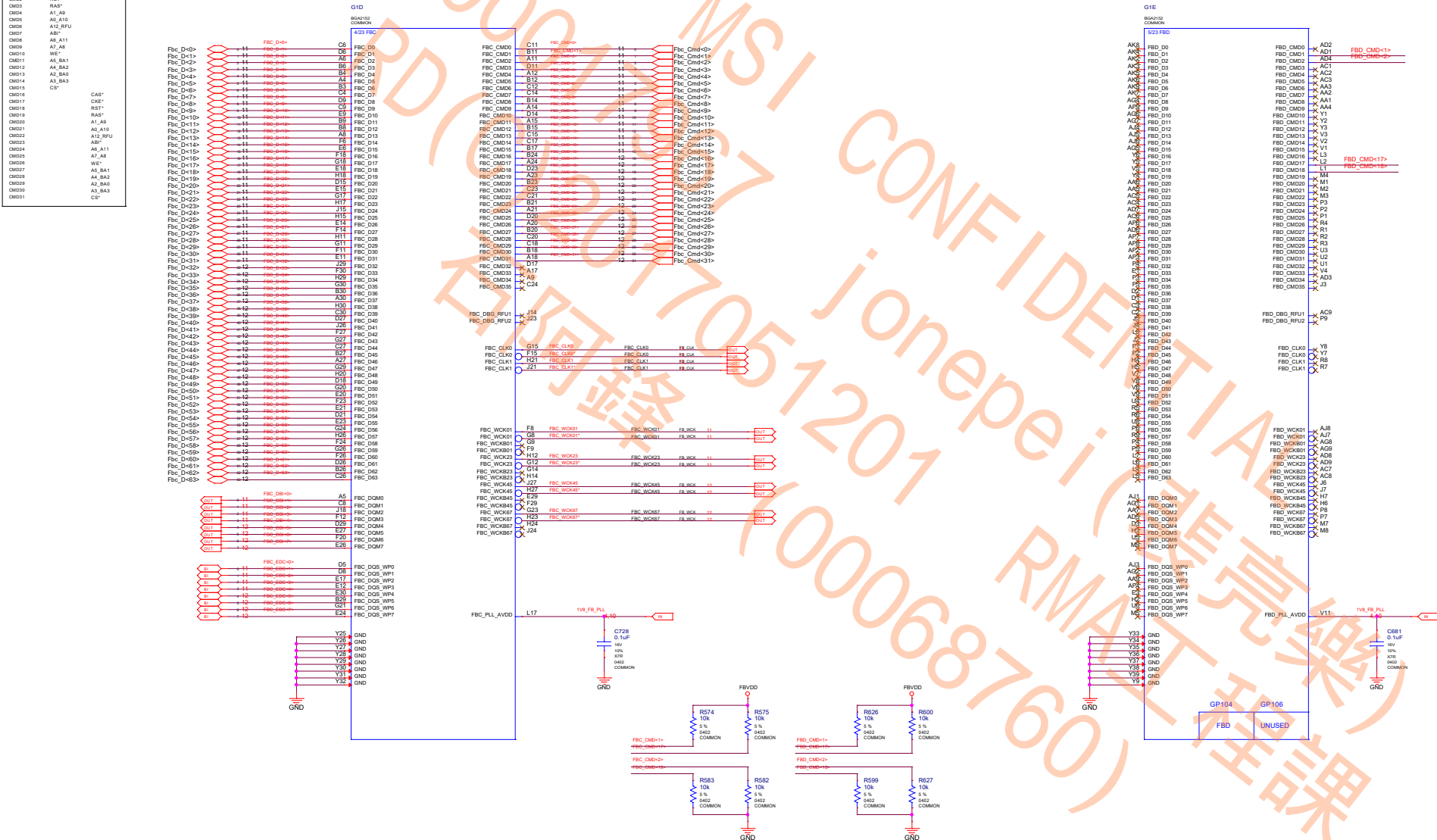


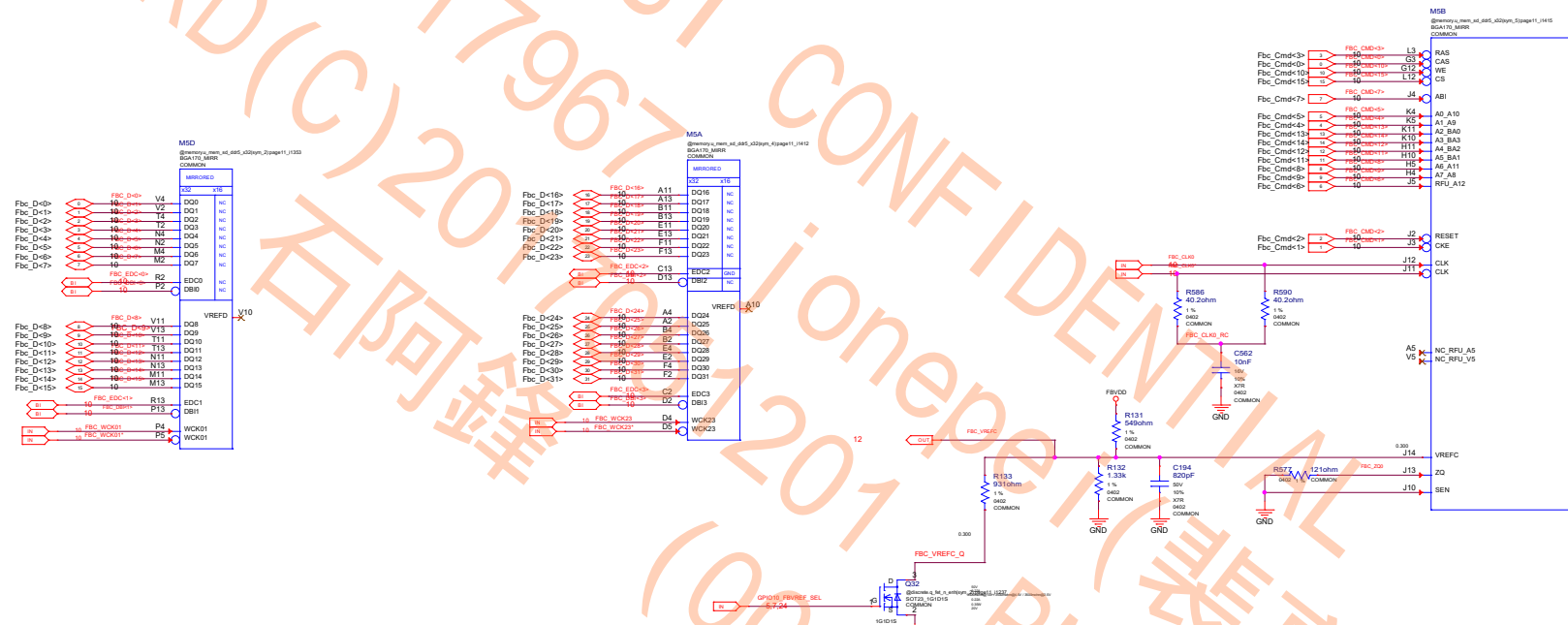


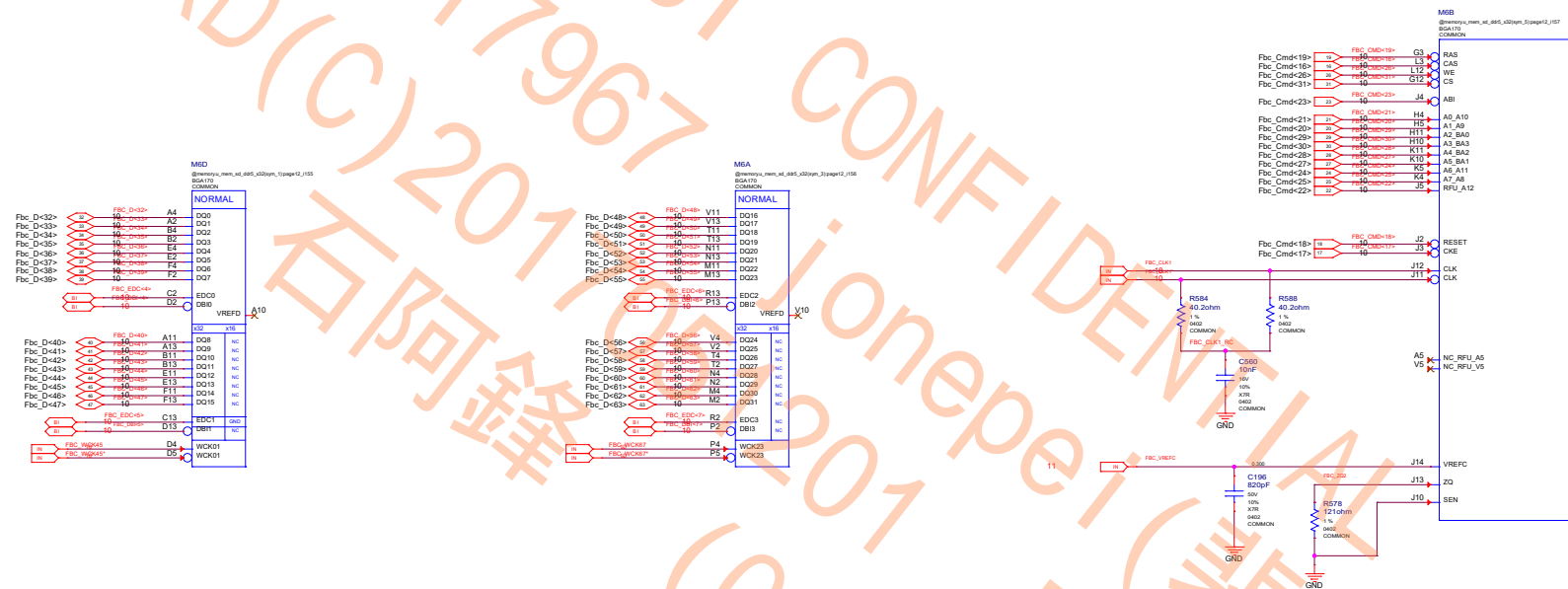


GDDR5 CMD Mapping


CMD	G-31	32-63
CM00	CAS*	
CM01	CKE*	
CM02	RS*	
CM03	RAS*	
CM04	A1_A8	
CM05	A9_A10	
CM06	A12_RFU	
CM07	AB*	
CM08	AB_A11	
CM09	A7_A8	
CM10	WE*	
CM11	AS_BA1	
CM12	AS_BA2	
CM13	A2_BA0	
CM14	A3_BA3	
CM15	CS*	
CM16		CAS*
CM17		CKE*
CM18		RS*
CM19		WE*
CM20	A1_A8	
CM21	A9_A10	
CM22	A12_RFU	
CM23	AB*	
CM24	AB_A11	
CM25	A7_A8	
CM26	WE*	
CM27	AS_BA1	
CM28	AS_BA2	
CM29	A2_BA0	
CM30	A3_BA3	
CM31	CS*	





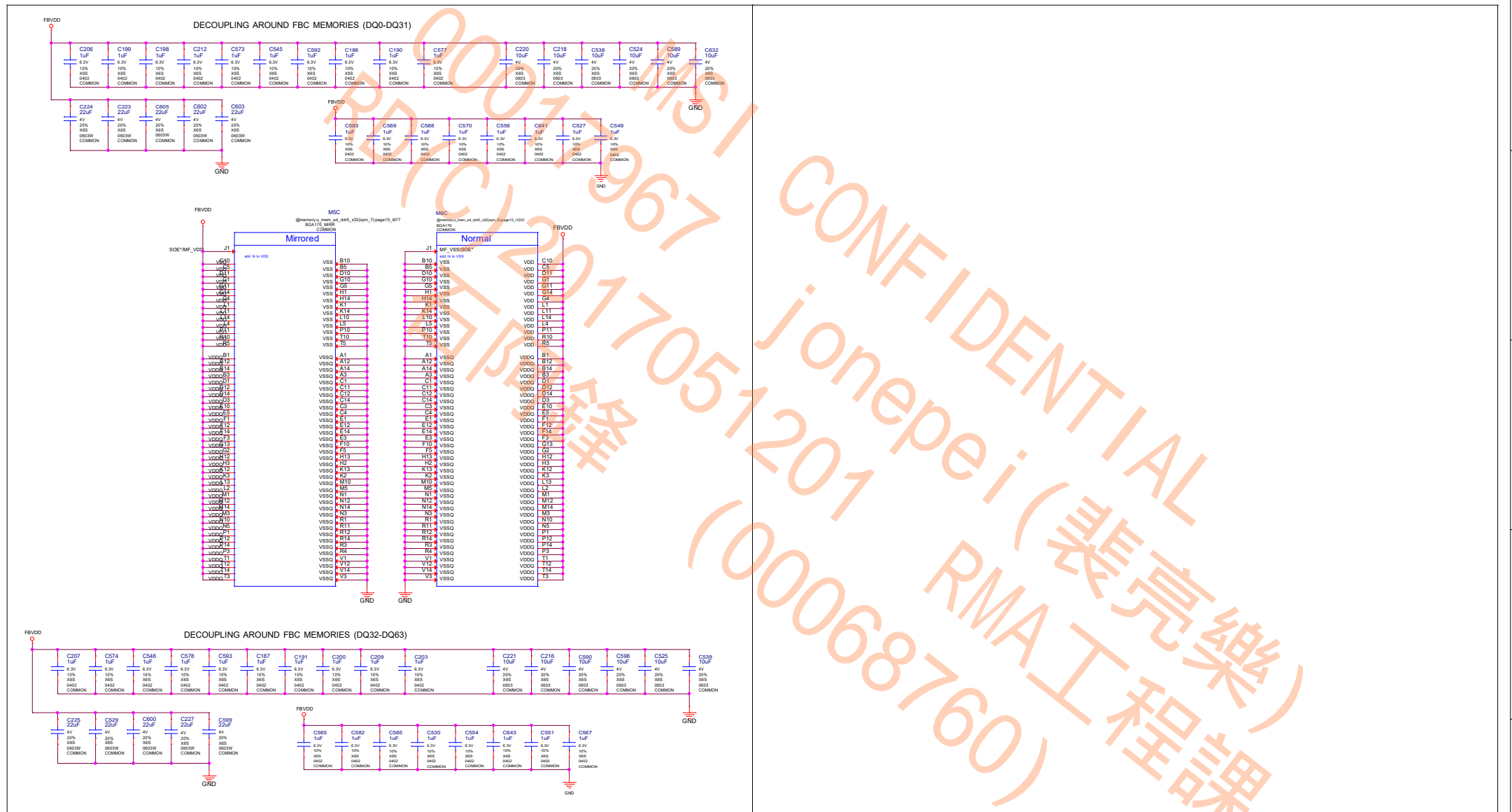


MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2017051201 RMA工程課
石阿鋒 (00068760)

	MICRO-STAR INT'L CO.,LTD		
	MS-V328		
	Size	Document Description	Rev
	Custom	13	7.0
Date: Friday, November 11, 2016			Sheet 13 of 38

MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2017051201 RMA工程課
石阿鋒 (00068760)

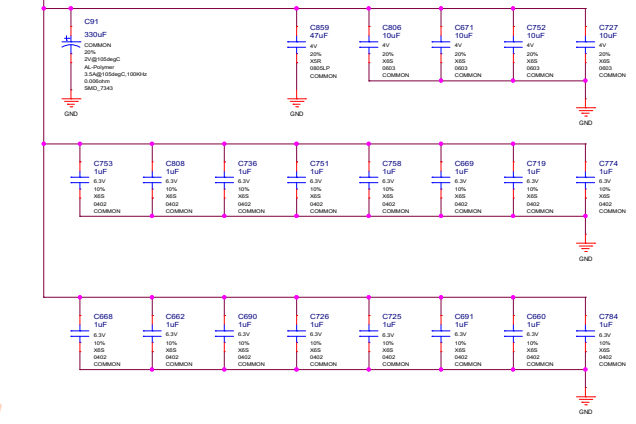
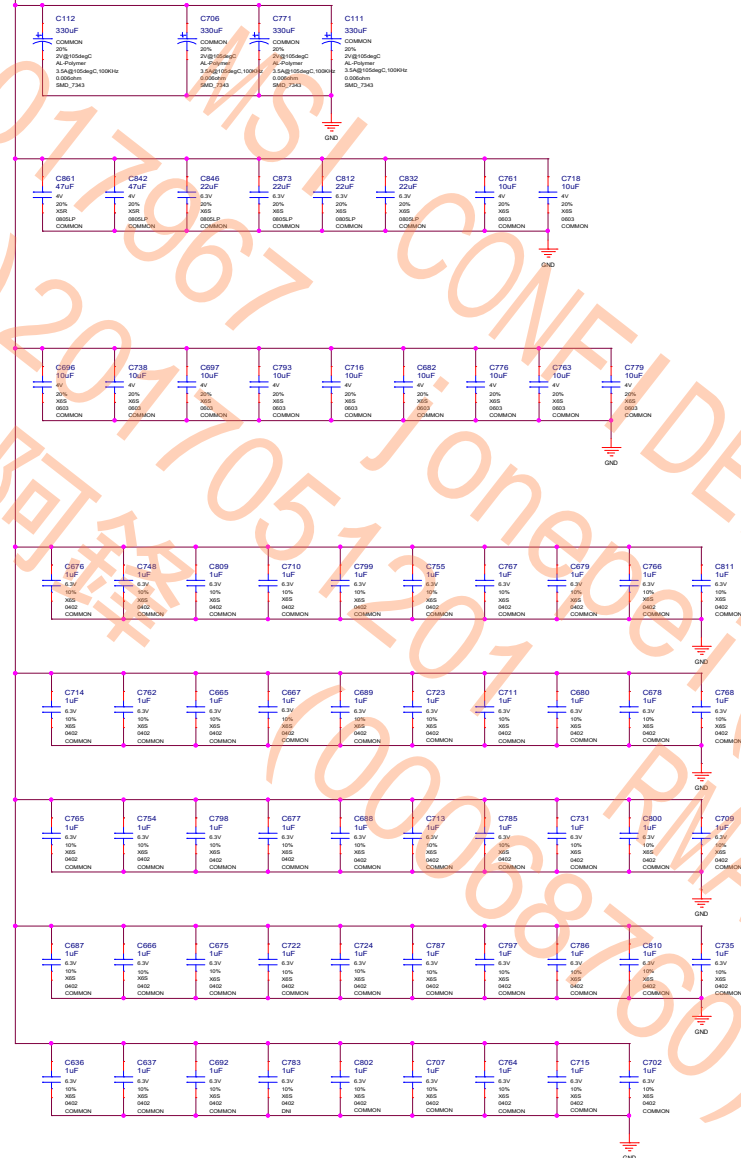
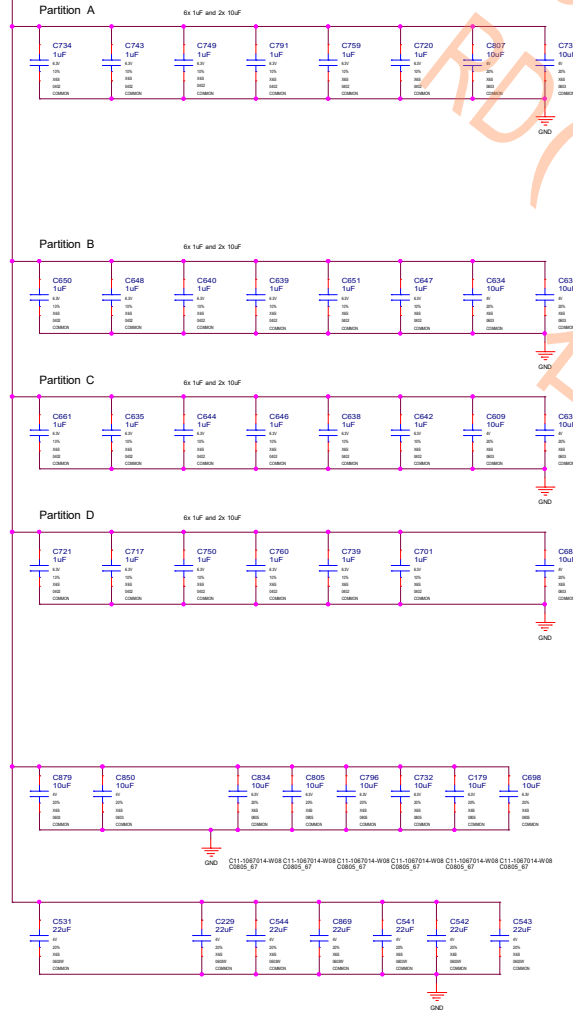
	MICRO-STAR INT'L CO.,LTD		
	MS-V328		
	Size	Document Description	Rev
	Custom	14	7.0
Date: Friday, November 11, 2016			Sheet 14 of 38



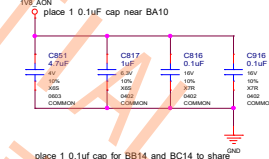
FBVDD

NVDD

NVDD

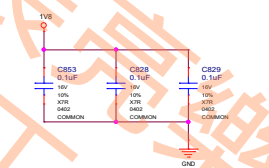


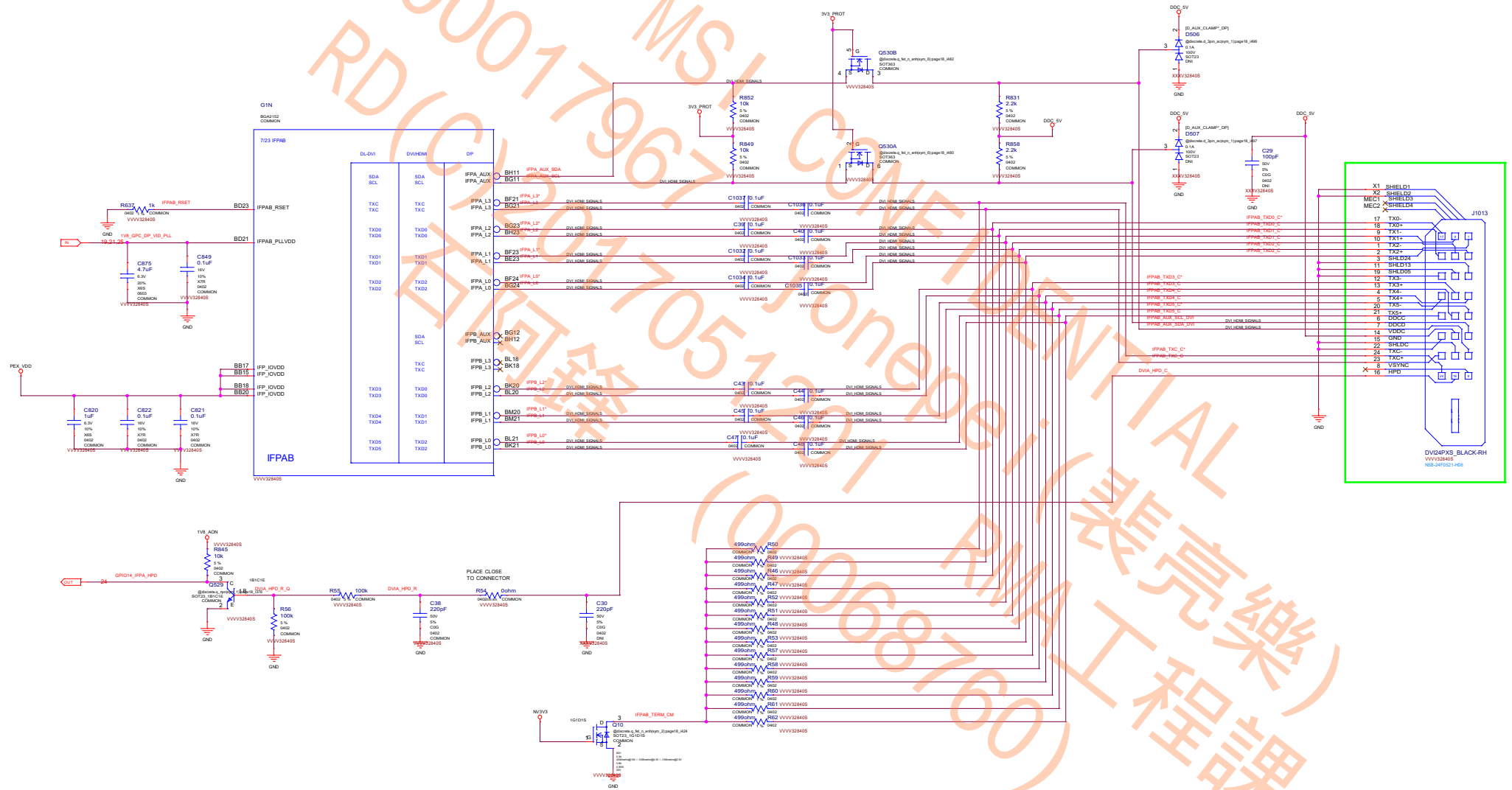
1V8_AON



place 1 0.1uF cap for B614 and B614 to share

1V8_MAIN

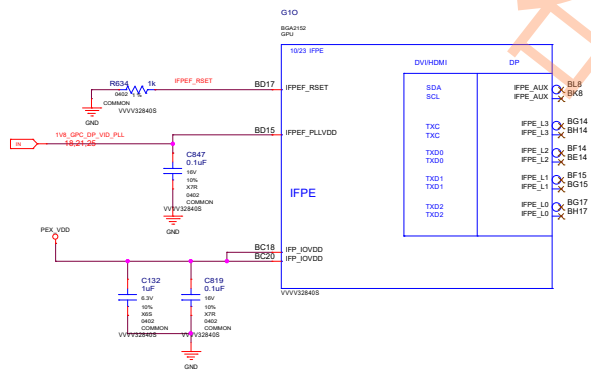


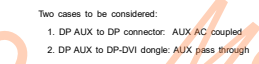


更換為單層無架高

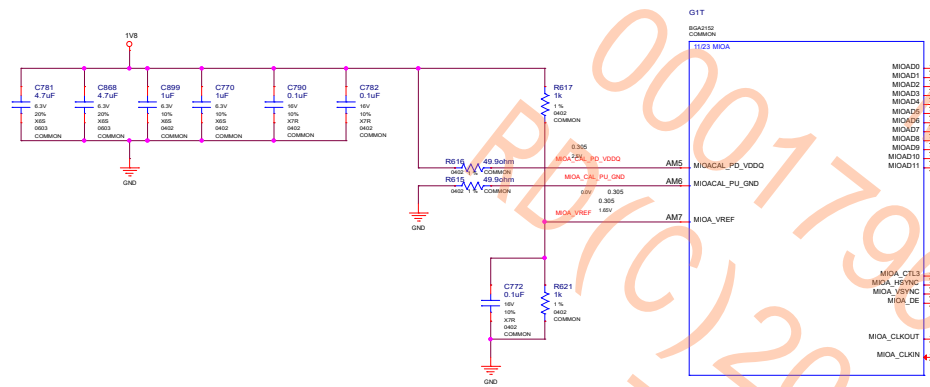
17ci203

MICRO-STAR INT'L CO., LTD			
MS-V328			
Size	Document	Description	Rev
Custom	18		7.0
Date:	Friday, November 11, 2016	Sheet	18 of 38

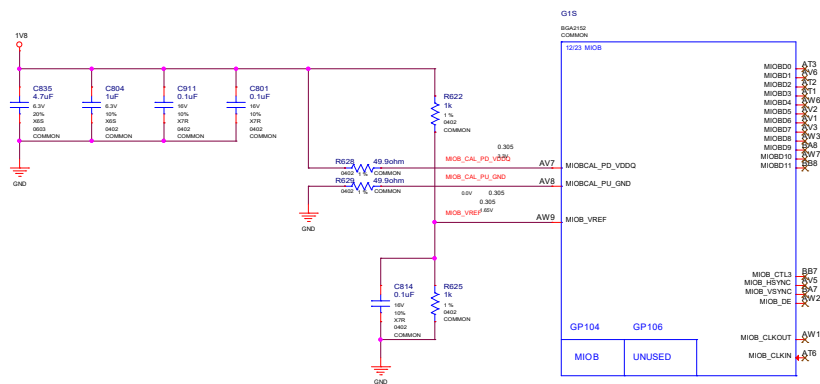




Remove DP J4



Pad Overlap R1042 & R1043



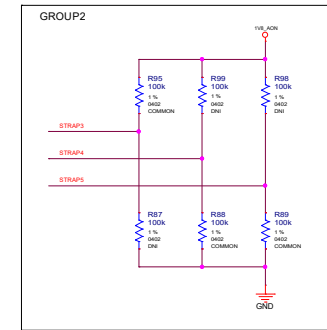
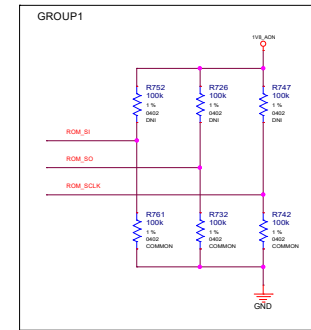
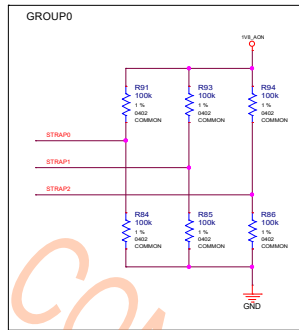
STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000
ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

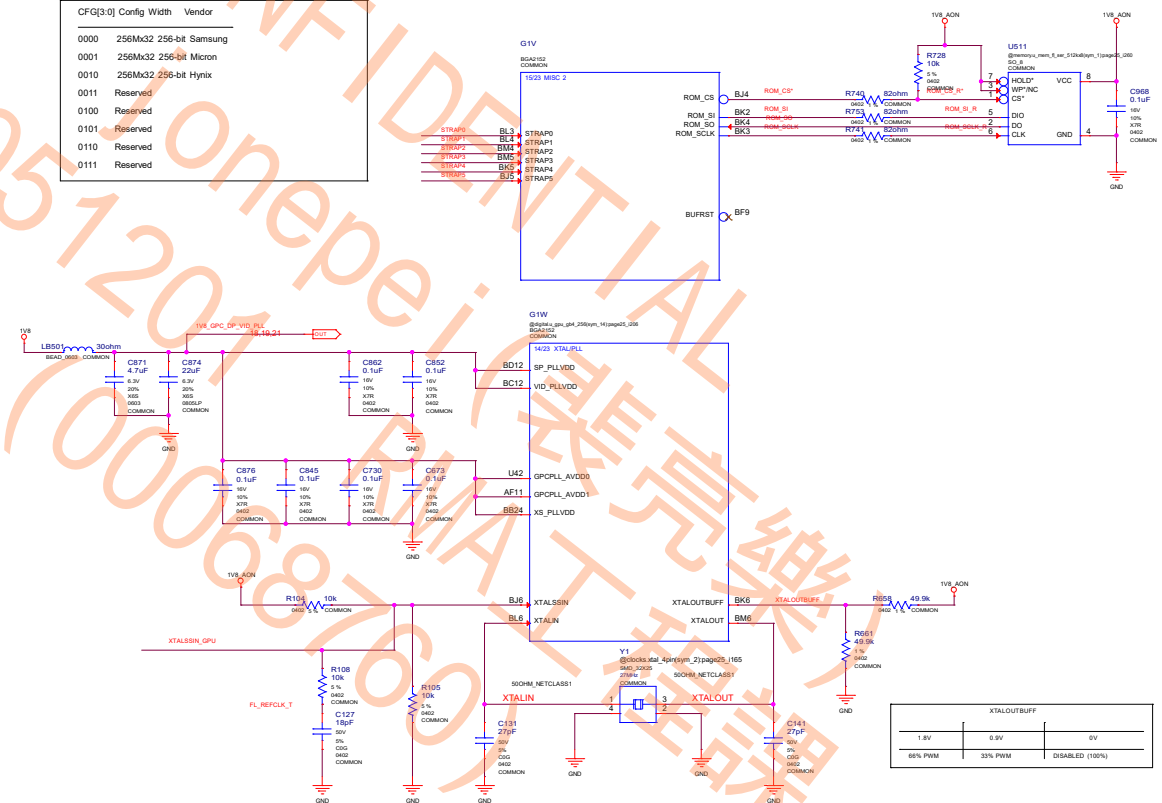
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



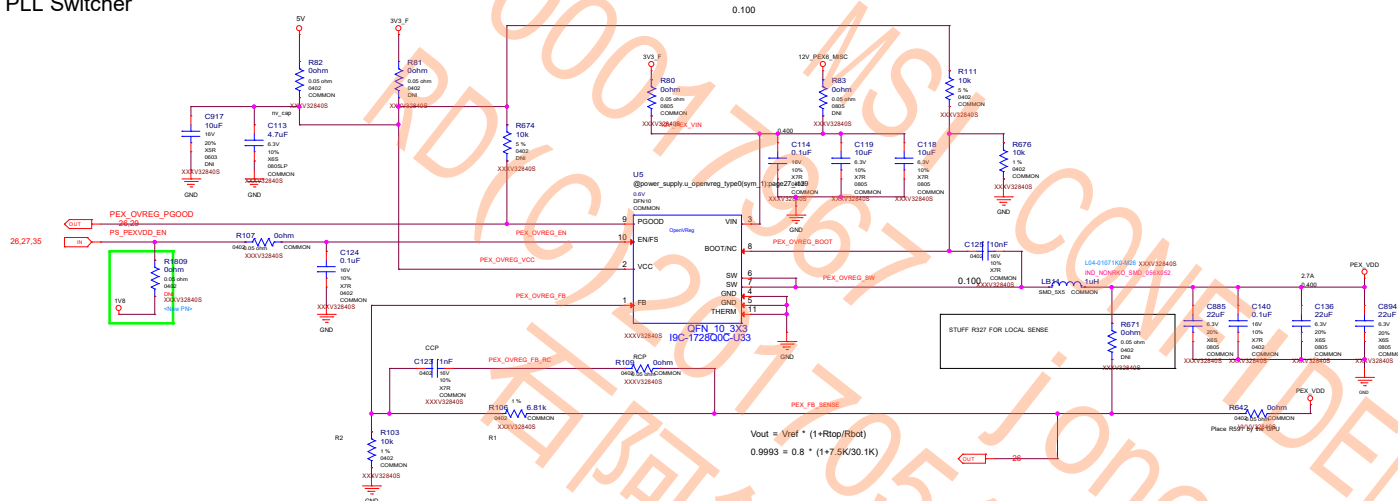
CFG(3:0)	Config	Width	Vendor
0000	256Mx32 256-bit Samsung		
0001	256Mx32 256-bit Micron		
0010	256Mx32 256-bit Hynix		
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		



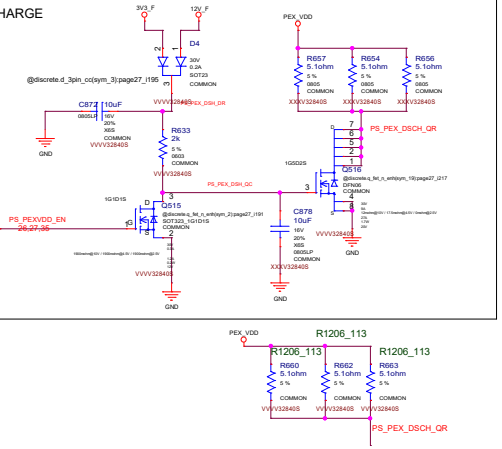
XTALOUTBUFF		
1.8V	0.9V	0V
88% PWM	33% PWM	DISABLED (100%)

MICRO-STAR INT'L CO.,LTD		
MS-V328		
Size	Document Description	Rev
Custom	25	7.0
Date:	Friday, November 11, 2016	Sheet 25 of 38

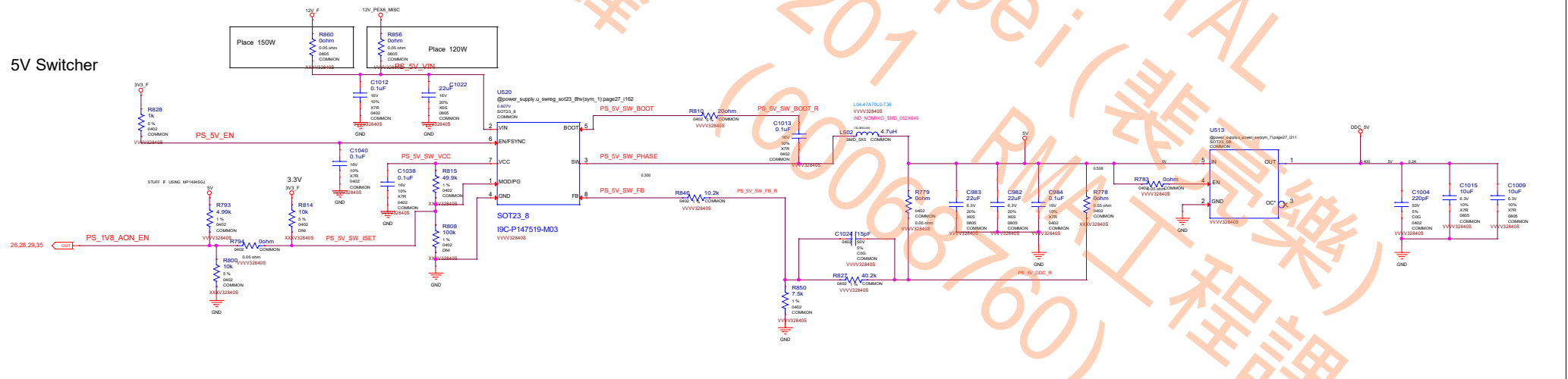
PEX PLL Switcher



PEX_VDD DISCHARGE

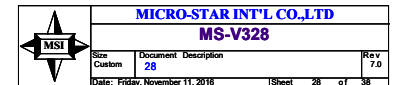
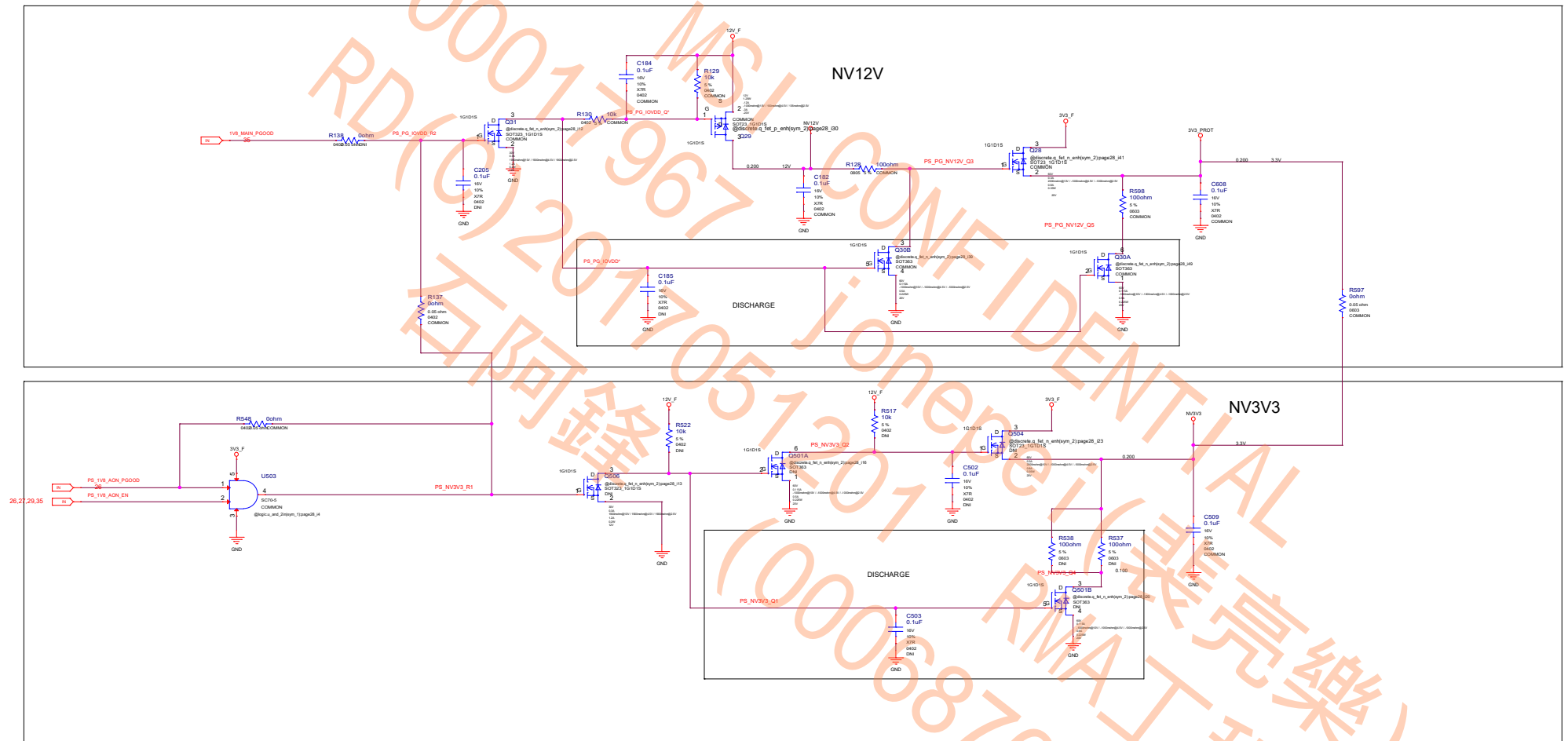


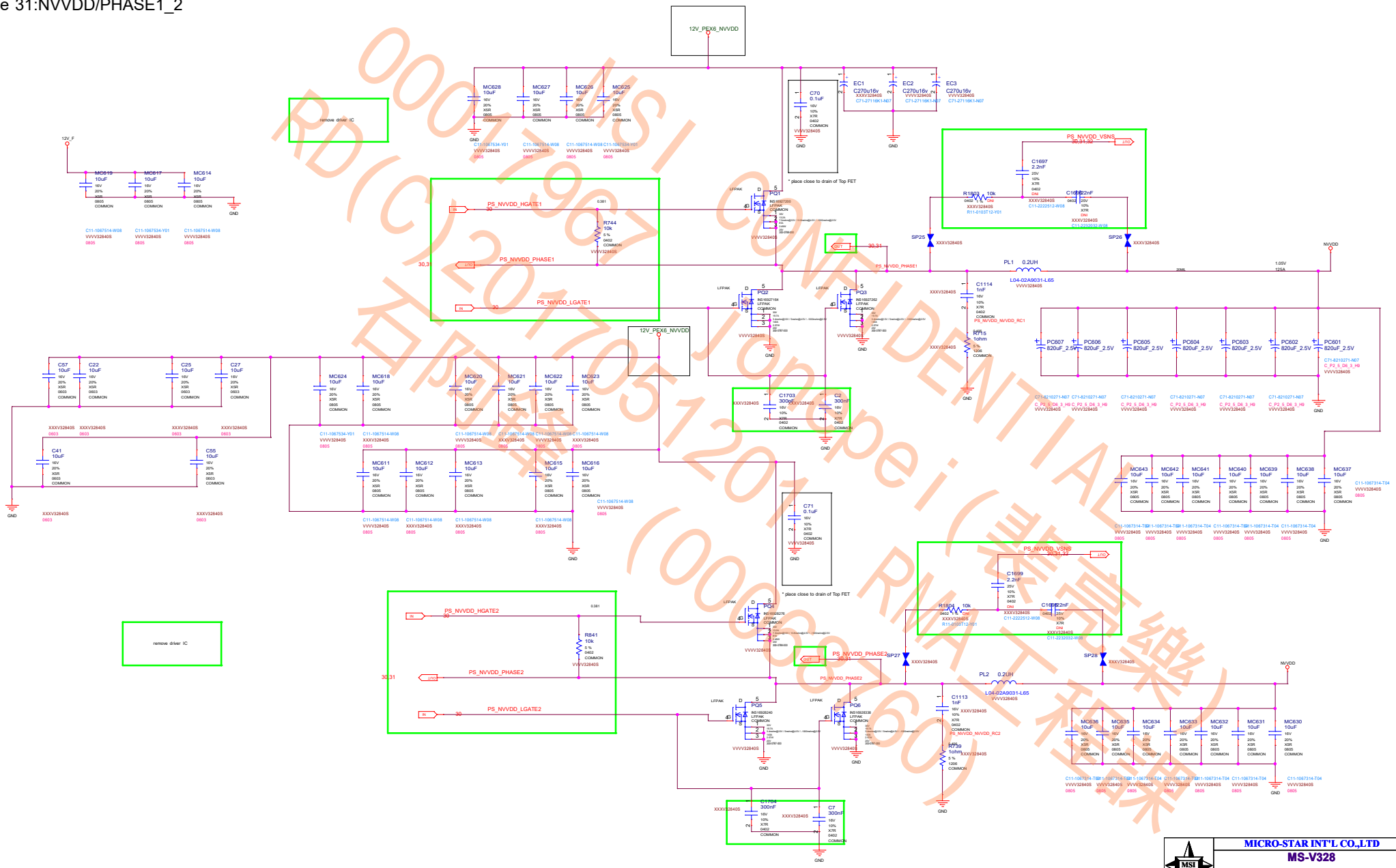
5V Switcher

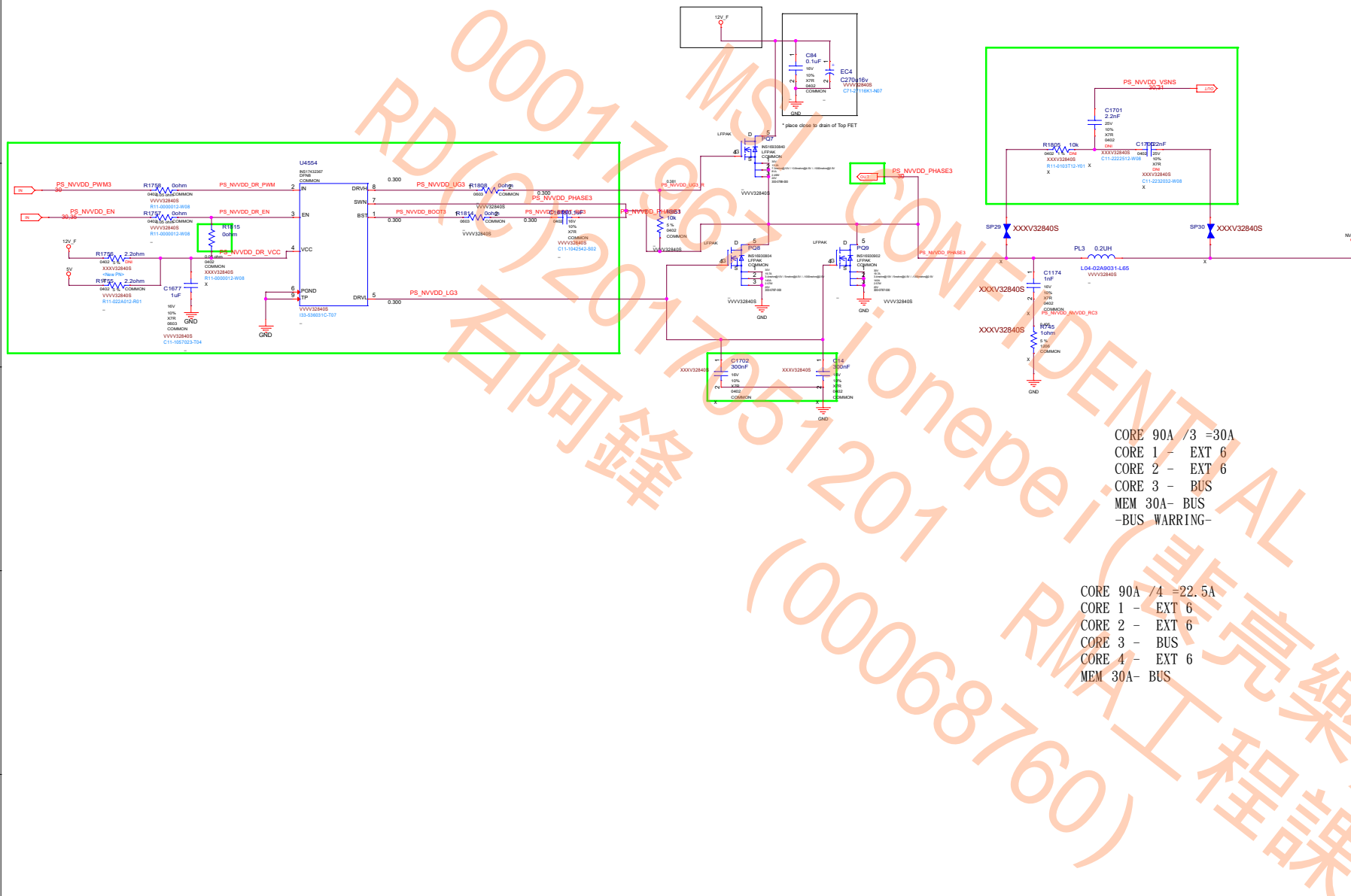



17ci203

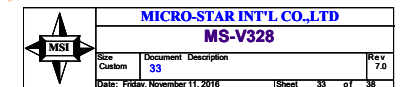
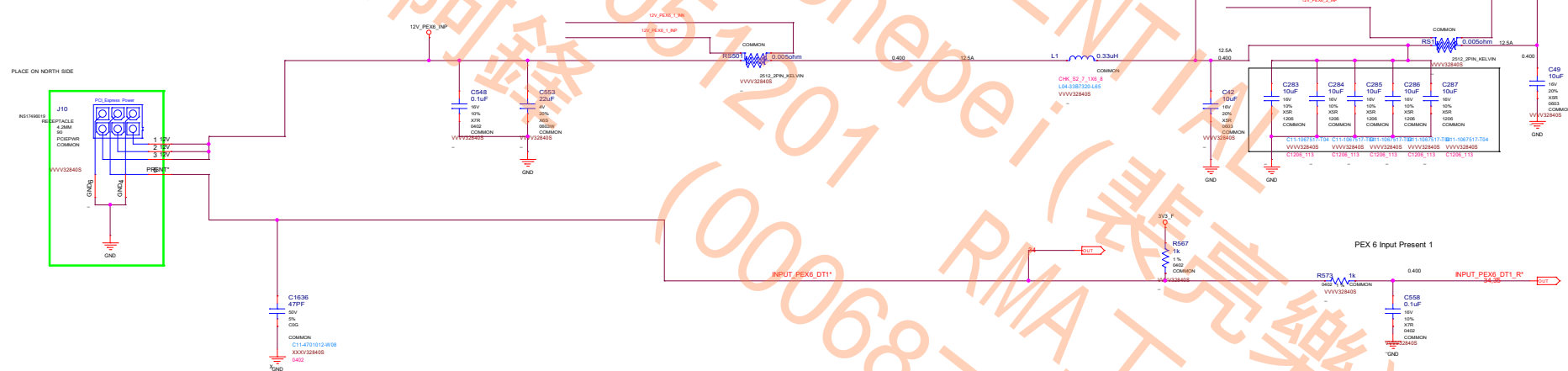
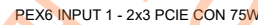
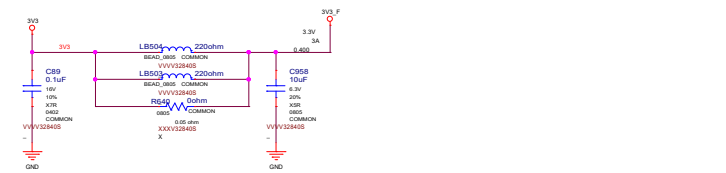
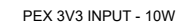
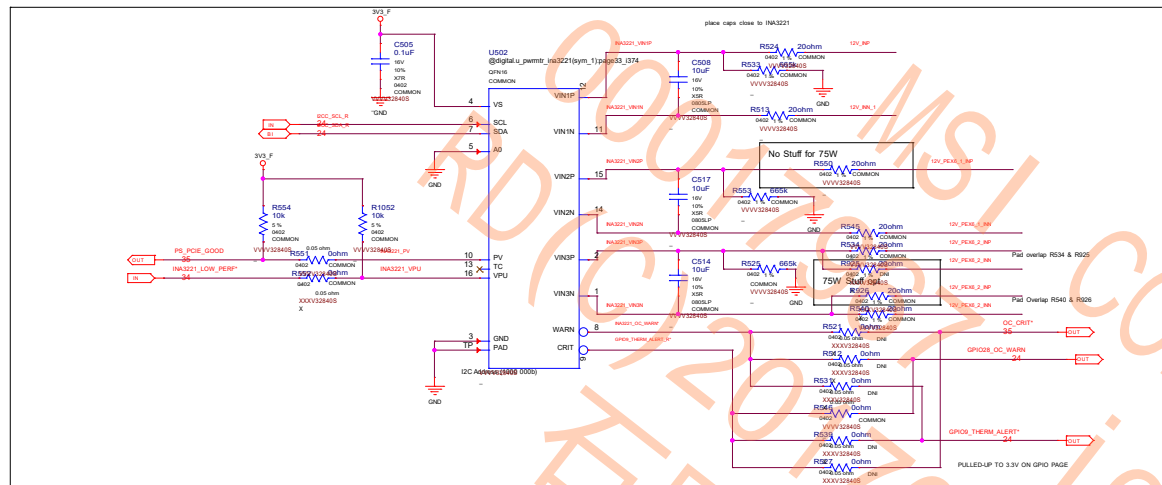
	MICRO-STAR INT'L CO., LTD		
	MS-V328		
	Size	Document Description	Rev
	Custom	27	7.0
Date: Friday, November 11, 2016		Sheet: 27	of 38





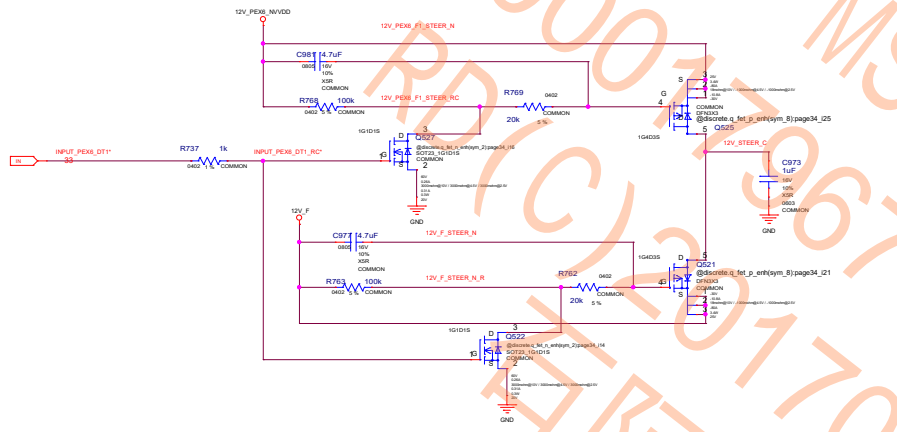


	MICRO-STAR INT'L CO.,LTD		
	MS-V328		
	Size Custom	Document Description NVDD/PHASE3_4	Rev 7.0
Date: Friday, November 11, 2016		Sheet 32 of 38	

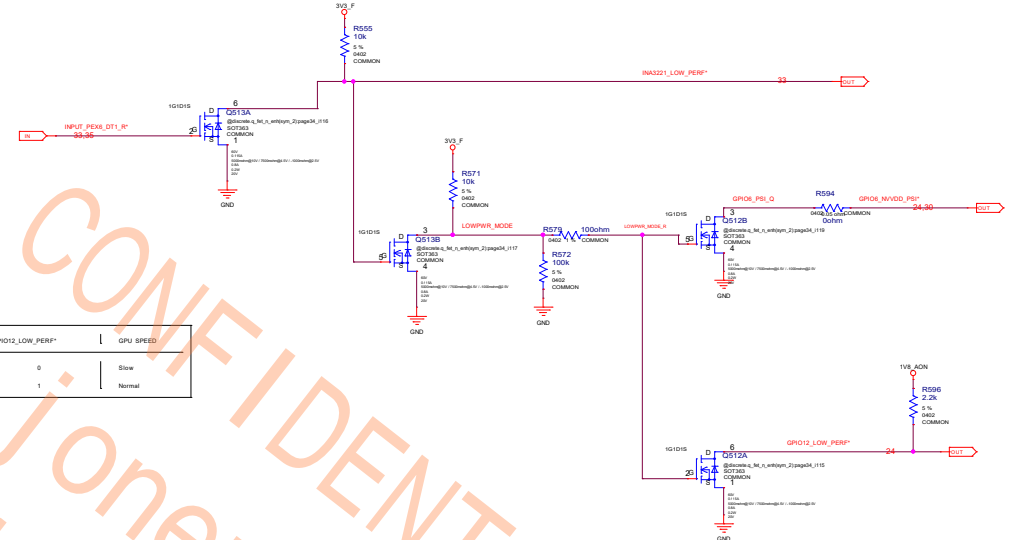


12V CURRENT STEERING (UNDER POWER BOOT):

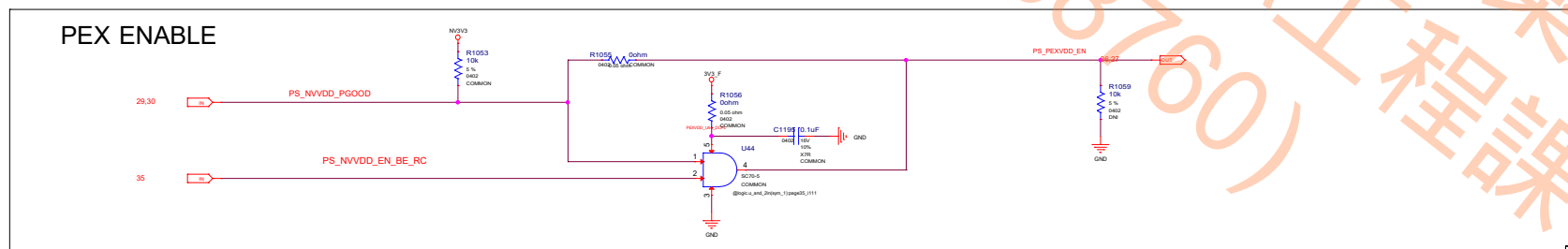
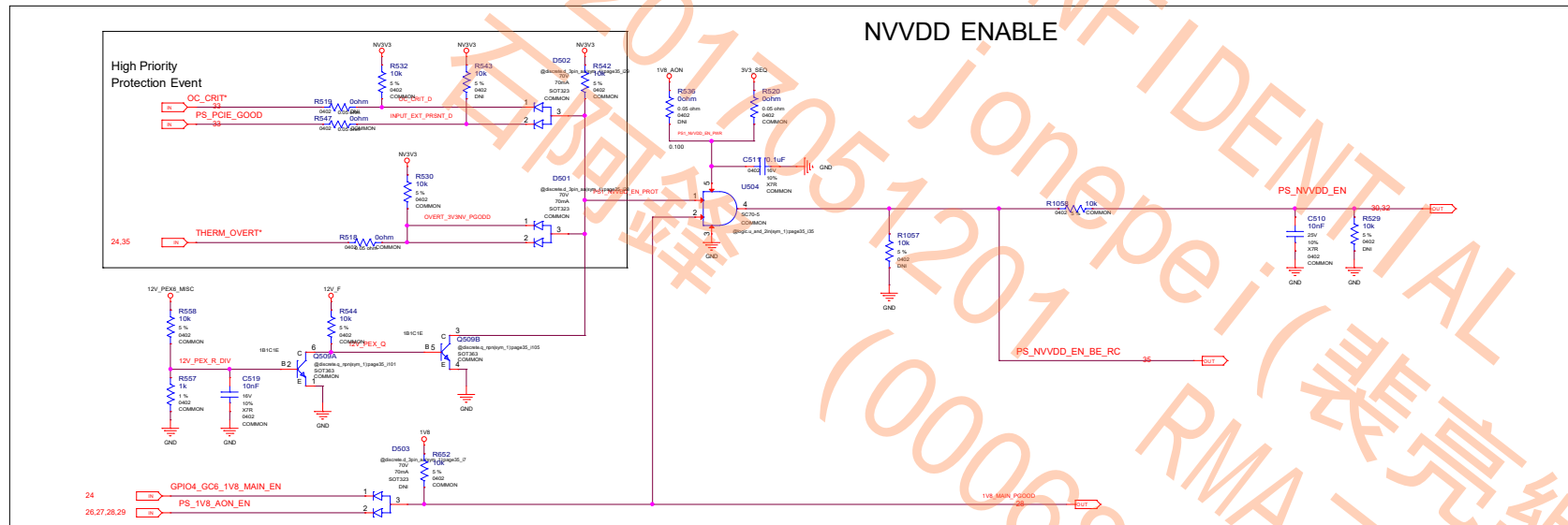
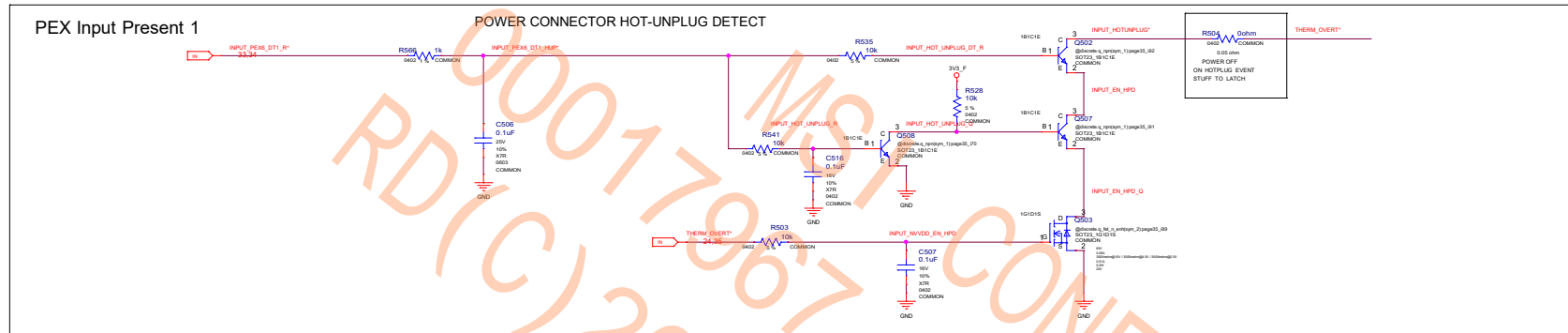
GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

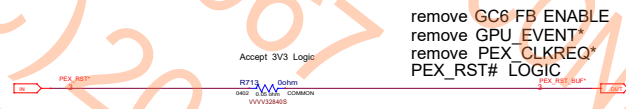


PEX Input - Power Level/PSI* Control



GeForce Logo LED

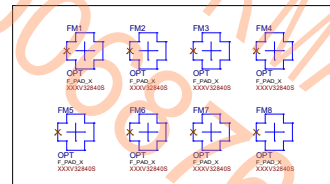
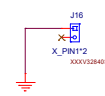
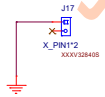
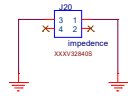
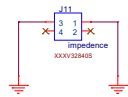
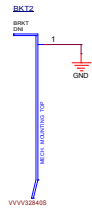




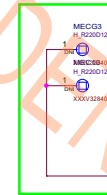
remove 5V LED NET

MICRO-STAR INT'L CO.,LTD			
MS-V328			
Size	Document	Description	Rev
Custom	36		7.0
Date: Friday, November 11, 2016		Sheet	36 of 38

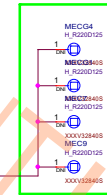
Brackets:



NVVDD MOS Holes Symbol




GPU Holes Symbol



Remove: MEC12/MEC13/MEC14/MEC15/MEC11/MEC8/MECG2/MECG1

Page: 18	DVI-D 與 螢幕 連接線
Page: 19	Remove DP
Page: 20	Remove DP
Page: 22	from HDMI change to DP
Page: 24	Remove gpio 24 DP HPD Remove Remove gpio 18 DP HPD remove LED NET gpio 17 , from HDMI change to DP HPD
Page: 27	將 1.8V to PEX-VDD convertor
Page: 29	將 0402 MLCC*2 for L side mos
Page: 30	change PWM to I32-9509POC-U33
Page: 31	remove phase1 & phase2 driver IC
Page: 32	change phase3 driver IC to I33-536031C-T07 remove phase4
Page: 33	Remove COALY 8-PIN 6-PIN 晶片 位置
Page: 36	remove 5V LED NET
Page: 37	Remove: MEC12/MEC13/MEC14/MEC15/MEC11/MEC8/MECG2/MECG1

				MICRO-STAR INT'L CO.,LTD			
				MS-V328			
Size	Custom	Document	Description	Rev			
	37			7.0			
Date: Friday, November 11, 2016				Sheet	38	of	38